XILINXPWR-079 (HPA-079)
TPS64203 Switching DC/DC Controller-Based Power Management Solution for Spartan™-3 Providing up to 3 A from V_{IN} = 5.0 V or 3.3 V

SUPPORTS:

- Spartan™-3 – supports PR213 at the following link: http://www-s.ti.com/sc/techlit/slva174.pdf

- Spartan™-II - board requires significant modification to support PR211 at the following link: http://www-s.ti.com/sc/techlit/slva172.pdf

- Spartan™-IIE - board requires significant modification to support PR212 at the following link: http://www-s.ti.com/sc/techlit/slva173.pdf

FEATURES:

- Tiny SOT-23 switching DC/DC controller, U2, delivers up to 3 A at low cost.
- Easily customizable design allows for maximum cost control by:
  - Sizing Q3 for the amount of current up to 3 A to meet the application's I_{CCINT} requirement,
  - Omitting current sense resistor R4 and connecting ISNS to the drain of Q3,
  - Selecting the linear regulator from the TPS79xxx family to meet the application's I_{CCO} requirement.
- In-rush current (for charging decoupling capacitors and FPGA start-up) that places a demand on the input power supply is minimized by the use of the:
  - External supervisory (SVS) IC, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
  - Integrated soft-start of U2
  - Soft-start circuit consisting of the external PMOS transistor Q4 and supporting passive components to provide 10 ms rise time for V_{CCO}
  - Sequential sequencing of V_{CCINT}, V_{CCAUX} then V_{CCO}
    - the discrete SVS circuit formed by bipolar transistors Q1 and Q2 and supporting passives enables the V_{CCAUX} regulator, U3
    - V_{CCAUX} enables the V_{CCO} regulator, U4
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.

- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps64203.pdf, http://focus.ti.com/lit/ds/symlink/tps78601.pdf, http://focus.ti.com/lit/ds/symlink/tps79401.pdf, and http://focus.ti.com/lit/ds/symlink/tlc7705.pdf.
- Link to application note SLVA156 http://focus.ti.com/lit/an/slva156/slva156.pdf for more details on the soft-start circuit.
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations when using linear regulators.
- Link to application note SLVA160 http://focus.ti.com/lit/an/slva160/slva160.pdf for guidance on selecting a different option from the TPS642xx family.
- Link to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf when using 3.3-V JTAG ports.

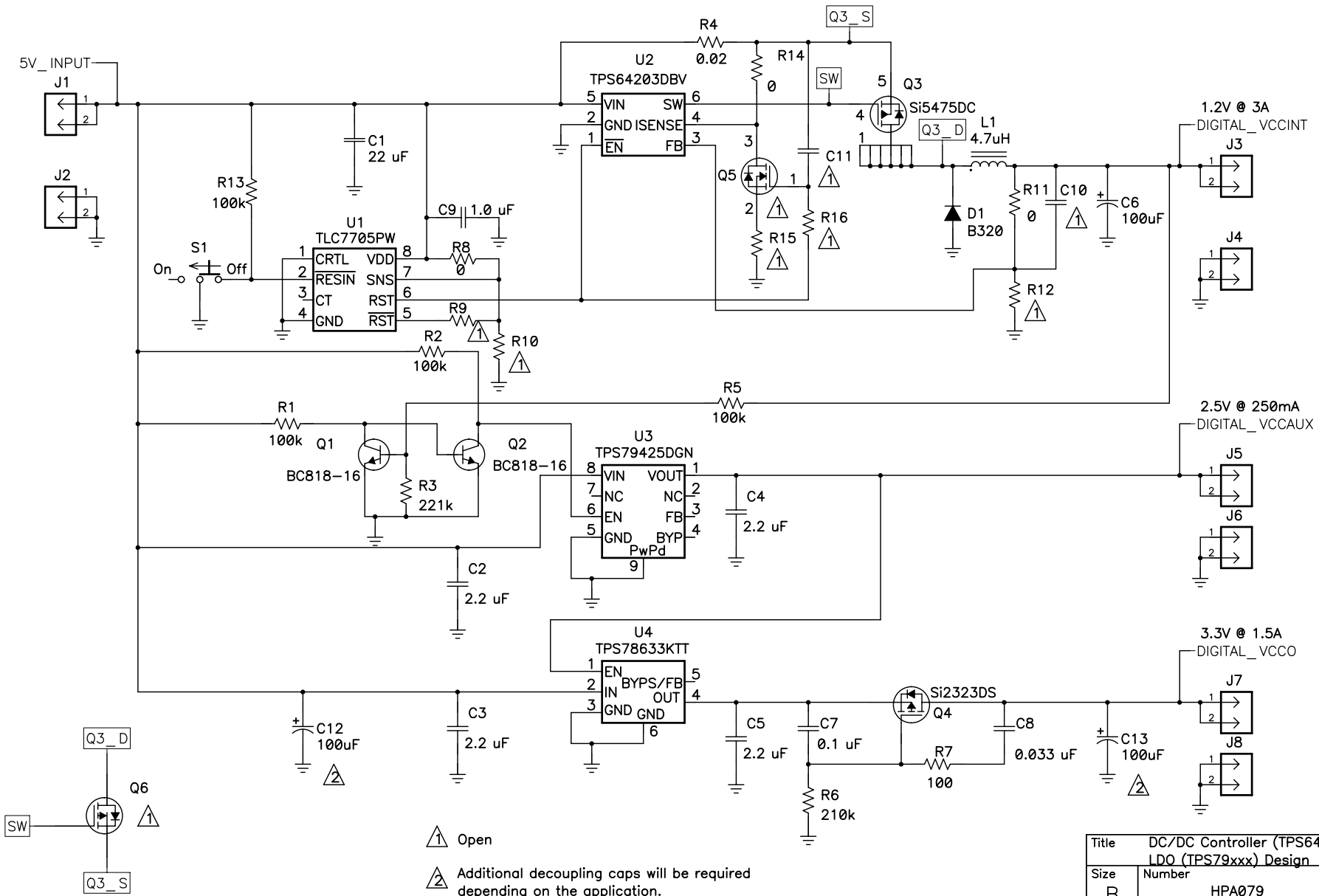
IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads all at once.
- **V_{CCO} minimum ramp time:** Met by Q4 soft-start circuit
- **Power Dissipation/Thermal Issues:**
  - Diode D1 in SMA package can only support 3A for ambient temperatures below 35 C. This diode will need to be increased to an SMC package or DDPAK package in order to provide the power dissipation necessary for higher ambient temperature. Refer to the diode's datasheet for thermal specifications.
  - Refer to the application section of the linear regulator datasheet for maximum power dissipation at different ambient conditions as well as guidance on sizing the ground plane area underneath the package for heatsinking.
- **Designing with the TPS64203:**
  - The TPS64203 controller has limited current to drive the gate of the PMOS transistor, Q3. To ensure proper operation of the controller, a PMOS transistor with a maximum total gate charge, Q_g, of less than 50 nC is required.
  - Omitting current sense resistor R4 and connecting ISNS to the drain of Q3, thereby using the R_{DSon} of Q3 as the current sense, results in an effective, but slightly less accurate, current limit function.
- **Soft Start Circuitry:**
  - PMOS transistor Q4 should be selected so that its threshold voltage, V_{TH}, is at least 0.9 V below the V_{CCO} voltage or lower (e.g., $V_{TH} \leq 3.3\ V - 0.9\ V = 2.4\ V$). In addition, the transistor's R_{DSon} should be low enough when driven by the output of the linear regulator so that the voltage drop across

the transistor at maximum current (e.g., $I_{CCINTmax}$*R_{DSon}) does not cause V_{CCO} to fall below its -5% tolerance.
    - The drain of Q4 needs at least 10 uF of total capacitance in order for the soft-start circuit to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for the V_{CCO} rail of the FPGA will most likely meet this requirement.
- **Layout:** The 1.0 uF capacitor, C7, should be placed as close as possible between VDD and GND of the TLC77xx SVS IC.
- **Modifications:**
    - CT of TLC7705 is not connected, but can be used with a capacitor to add a delay between the 5 V rail coming up and RST = /EN of TPS64203.
    - Adapt for 3.3V supply by:
        - Omitting U4 circuit,
        - Replacing TLC7705 with TLC7733.
    - For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).
- **3.3V Configuration**
    - The Spartan-3 FPGA configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configurations and JTAG input pins, through the FPGA, to the V_{CCAUX} power rail. Therefore, please refer to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf for implementation guidance.

QUESTIONS?

- Send an email to **fpgasupport@list.ti.com**


5V_INPUT
J1
J2
C1
22 uF
R13
100k
U1
TLC7705PW
CRTL
RESIN
CT
GND
VDD
SNS
RST
RST
S1
On
Off
C9
1.0 uF
R8
0
R9
R10
R2
100k
R1
100k
Q1
BC818-16
Q2
BC818-16
R3
221k
R5
100k
U2
TPS64203DBV
VIN
GND
EN
SW
ISENSE
FB
R4
0.02
R14
0
Q3_S
SW
Q3
Si5475DC
Q3_D
L1
4.7uH
C11
Q5
R16
R15
D1
B320
R11
0
C10
C6
100uF
R12
1.2V @ 3A
DIGITAL_VCCINT
J3
J4
U3
TPS79425DGN
VIN
NC
EN
GND
VOUT
NC
FB
BYP
PwPd
C4
2.2 uF
C2
2.2 uF
2.5V @ 250mA
DIGITAL_VCCAUX
J5
J6
U4
TPS78633KTT
EN
IN
GND
BYPS/FB
OUT
GND
C12
100uF
C3
2.2 uF
C5
2.2 uF
C7
0.1 uF
R6
210k
Si2323DS
Q4
R7
100
C8
0.033 uF
C13
100uF
3.3V @ 1.5A
DIGITAL_VCCO
J7
J8
Q3_D
Q6
SW
Q3_S
1 Open
2 Additional decoupling caps will be required depending on the application.
Title DC/DC Controller (TPS64203) and LDO (TPS79xxx) Design
Size B
Number HPA079
Rev A
Date 08/17/04
Drawn by
Filename hpa079a.sch
Sheet of

Filename: HPA079A_bom.xls

Date: 08/17/2004

HPA079A BOM

COUNT	RefDes	Description	SIZE	MFR	Part Number
1	C1	Capacitor, Ceramic, 22-uF, 10-V, X5R, 10%	1210	muRata	GRM32ER61A226KA65
0	C10, C11	Capacitor, Ceramic, xx-uF, xx-V	603		
4	C2, C3, C4, C5	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
3	C6, C12, C13	Capacitor, Tantalum, 100-uF, 10-V, 95-milliohm, 20%	7343 (D)	Vishay	594D107X0010D2T
1	C7	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E104KA01
1	C8	Capacitor, Ceramic, 0.033-uF, 16-V, X7R, 10%	603	muRata	GRM188R71C333KA01
1	C9	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
1	D1	Diode, Schottky Barrier Rectifier, 3-A, 20-V	SMA	Diodes Inc.	B320A
8	J1 - J8	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 4.7-uH, 4.5-A, 2-milliohm	0.484 x 0.484	Coilcraft	MSS1260-472MX
2	Q1, Q2	Bipolar, NPN, 30-V, 800-mA, 310-mW	SOT23	Vishay	BC818-16
1	Q3	MOSFET, P-ch, 20V,4.8-A, 76-milliohm	1206-8	Vishay	Si5475DC
1	Q4	MOSFET, P-ch, -20 V, 4 A, 51 milliohm	SOT23	Vishay	Si2323DS
0	Q5	MOSFET, N-ch	SOT23		
0	Q6	MOSFET, P-ch	SOT23		
4	R1, R2, R5, R13	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	603	Std	Std
1	R3	Resistor, Chip, 221k-Ohms, 1/16-W, 1%	603	Std	Std
1	R4	Resistor, Chip, 0.02-Ohms, 1/4-W, 1%	1210	Std	Std
1	R6	Resistor, Chip, 210k-Ohms, 1/16-W, 1%	603	Std	Std
1	R7	Resistor, Chip, 100-Ohms, 1/16-W, 1%	603	Std	Std
3	R8, R11, R14	Resistor, Chip, 0-Ohms, 1/16-W, 5%	603	Std	Std
0	R9, R10, R12, R15, R16	Resistor, Chip, xx-Ohms, 1/16-W	603		
1	S1	Switch, 1P2T, Slide, PC-mount, 200-mA	0.46 x 0.16	E_Switch	EG1218
1	U1	IC, Voltage Supervisor, Micropower	TSSOP-8	TI	TLC7705PW
1	U2	IC, Step-Down Controller	SOT23-6	TI	TPS64203DBV
1	U3	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, 2.5V	MSOP 8	TI	TPS79425DGN
1	U4	IC, Ultra Low-Noise, High PSRR, Fast RF 1.5A LDO Linear Regulator	DDPAK-5	TI	TPS78633KTT
1	--	PCB, 2.7 In x 2.45 In x 0.062 In		Any	HPA079

Notes:

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants.
   Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
   All other components can be substituted with equivalent MFG's components.

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